REMARKS

Claims 1, 2, 4-9, 11-14, and 29-33 are all the claims pending in the application. Claims 1, 2, 4-9, 11-14, and 29-33 stand rejected on prior art grounds. Applicants respectfully traverse these rejections based on the following discussion.

I. The Prior Art Rejections

Claims 1, 6-8, and 13-14 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Dawson et al. (5,963,803), hereinafter "Dawson." in view of Sakurai et al., hereinafter "Sakurai" (2001/0052648). Claims 1-2, 4-9, and 11-14 stand rejected under 35 U.S.C. §103(a) as unpatentable over Hellig et al., hereinafter "Hellig" (6,696,334) in view of Sakurai. Applicants respectfully traverse these rejections based on the following discussion.

A. The Rejection Based on Dawson and Sakurai

Applicants respectfully submit that none of the prior art of record teach or suggest the claimed structure where the "silicide regions are larger in said first-type transistors than in said second-type transistors" as defined by independent claims 1 and 8. With the invention, a space is formed under the spacer (by pulling back the oxide liner horizontally towards gate poly). Silicide is formed on the silicon in this opening (marked as silicide extension). Because the silicide is formed in a narrow vertical spacing, its thickness is thinner than normally formed silicide and is self-limited to the opening. Silicide has to be thin to prevent punch through (a short or high leakage between silicide and channel). The oxide liner under the silicon nitride spacer has different thicknesses so the amount of pullback (or undercut) is different between the different types of transistors.

Such is not the case with Dawson which utilizes consistently sized silicide on the transistors. More specifically, Dawson only briefly mentions generalized silicide processing in

the paragraph appearing in column 8, line 58-column 9, and line 9. Dawson does not provide any indication that different types of transistors will receive different sized silicide regions. Sakurai only forms silicide 107b under one of the two transistors (Figure 16) and does not change silicide 7b between the transistors. Therefore, no prior art of record teaches that both transistors should have silicide between the spacers and the substrate, and that this silicide should be different between the different types of transistors.

In other words, Dawson teaches that both types of transistors should receive similar silicide portions and Sakurai alters this teaching by providing that the silicide can be removed from one type of transistor. Neither reference suggests that when the silicide is included in both types of transistors, it should have a different size for one type of transistor when compared to the other. Further, the claims have been amended, above, two more clearly identify that each of the two types of transistors includes silicide regions.

The claimed invention forms a shallow silicide in the PFET extension to again reduce extension resistance. This is achieved by forming a recess in the TEOS layer under the PFET gate sidewall spacer. For example, some cobalt can be sputtered into the recess to form a very shallow silicide. As a result of the relatively fast boron diffusion, the extension of the PFET is relatively deeper and the formation of the shallow silicide in the PFET extension will not increase leakage. The size of the recess is modulated by the oxide thickness under the spacer nitride. The thicker the oxide, the larger the recess will be. A thicker oxide is formed under the PFET spacers than that under NFETs, hence a larger recess and larger silicide is formed for the PFETs. Therefore, the silicide region under the PFET devices is longer and closer to the gate conductor than the silicide region under the NFET devices (see paragraph 25 of the application).

Further, Applicants continue to disagree with the position in the Office Action regarding Sakurai disclosing "silicide regions between portions of said sidewall spacers and said substrate" as defined by independent claims 1 and 8. The Office Action is apparently relying upon the somewhat vague positioning of items 107b with respect to the gate oxide 5 within Figure 16 of Sakurai for its contention that the silicide 107 is below the spacers 9. It is Applicants position that item 107b does not extend under spacers 9 in Figure 16, which is apparently contrary to the

interpretation of the drawings that is presented in the Office Action. Applicants' interpretation of Figure 16 is supported by paragraph 86 of Sakurai, which explains that the silicide layer 107b is formed on the whole surface of the heavily doped diffusion region 4b which is not covered with sidewall insulating layer 9 and isolating oxide film 3. Thus, in Sakurai, the silicide regions 107b form on areas outside those protected by the spacers 9 and do not formed below the spacers and between portions of the sidewall spacers and substrate as defined by independent claims 1 and 8. Therefore, paragraph 86 of Sakurai explains that the silicide regions 107b do not extend under the gate oxide 5 or under the spacers 9.

It is Applicants' position that silicide regions 107b are not formed below the spacers 9 as explained in paragraph 86 of Sakurai. Further, silicide regions 7a and 7b are formed at the bottom of contacts 13 and are not formed between the sidewall spacers 9 and the substrate 2 and have nothing to do with the claimed invention. Therefore, the fact that Sakurai uses silicide regions 107b for one transistor and does not utilize such silicide regions for another transistor is irrelevant to the claimed invention, as the claimed invention is referring to different silicide regions and more particularly to silicide regions that are between portions of the sidewall spacers and the substrate.

Therefore, even if one ordinarily skilled in the art had combined Dawson with Sakurai as suggest in the Office Action, the proposed combination would not teach or suggest the claimed structure where the "silicide regions are larger in said first-type transistors than in said second-type transistors" as defined by independent claims 1 and 8 especially since the silicide regions comprise "regions between portions of said sidewall spacers and said substrate."

Thus, Applicants submit that independent claims 1 and 8 are not taught or suggested by the prior art of record and independent claims 1 and 8 are patentable over the prior art of record. Further, dependent claims 6, 7, 13, and 14 are similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also by virtue of the additional features of the invention they define. In view of the foregoing, Applicants respectfully request that the Examiner reconsider and withdrawn this rejection as it applies to claims 1, 6-8, 13, and 14.

B. The Rejection Based on Hellig and Sakurai

Applicants respectfully submit that none of the prior art of record teach or suggest the claimed structure where the "silicide regions are larger in said first-type transistors than in said second-type transistors" as defined by independent claims 1, 8, and 29. As mentioned above, with the invention, a space is formed under the spacer (by pulling back the oxide liner horizontally towards gate poly). Silicide is formed on the silicon in this opening (marked as silicide extension). Because the silicide is formed in a narrow vertical spacing, its thickness is thinner than normally formed silicide and is self-limited to the opening. Silicide has to be thin to prevent punch through (a short or high leakage between silicide and channel). The oxide liner under the silicon nitride spacer has different thicknesses so the amount of pullback (or undercut) is different between the different types of transistors.

Such is not the case with Hellig which utilizes consistently sized silicide on the transistors. More specifically, Hellig only briefly mentions generalized silicide processing in the paragraph appearing in column 1, lines 13-30. Hellig does not provide any indication that different types of transistors will receive different sized silicide regions. Sakurai only forms silicide 107b under one of the two transistors (Figure 16) and does not change silicide 7b between the transistors. Therefore, no prior art of record teaches that both transistors should have silicide between the spacers and the substrate, and that this silicide should be different between the different types of transistors.

In other words, at most Hellig teaches that both types of transistors should receive similar silicide portions and Sakurai alters this teaching by providing that the silicide can be removed from one type of transistor. Neither reference suggests that when the silicide is included in both types of transistors, it should have a different size for one type of transistor when compared to the other. Further, the claims have been amended, above, two more clearly identify that each of the two types of transistors includes silicide regions.

As explained above, Sakurai does not disclose "silicide regions between portions of said sidewall spacers and said substrate" as defined by independent claims 1, 8, and 29. The Office

Action is apparently relying upon the somewhat vague positioning of items 107b with respect to the gate oxide 5 within Figure 16 of Sakurai for its contention that the silicide 107 is below the spacers 9. It is Applicants position that item 107b does not extend under spacers 9 in Figure 16, which is apparently contrary to the interpretation of the drawings that is presented in the Office Action. Applicants' interpretation of Figure 16 is supported by paragraph 86 of Sakurai, which explains that the silicide layer 107b is formed on the whole surface of the heavily doped diffusion region 4b which is not covered with sidewall insulating layer 9 and isolating oxide film 3. Thus, in Sakurai, the silicide regions 107b form on areas outside those protected by the spacers 9 and do not formed below the spacers and between portions of the sidewall spacers and substrate as defined by independent claims 1, 8, and 29. Therefore, paragraph 86 of Sakurai explains that the silicide regions 107b do not extend under the gate oxide 5 or under the spacers 9.

Thus, it is Applicants' position that silicide regions 107b are not formed below the spacers 9 as explained in paragraph 86 of Sakurai. Further, silicide regions 7a and 7b are formed at the bottom of contacts 13 and are not formed between the sidewall spacers 9 and the substrate 2 and have nothing to do with the claimed invention. Therefore, the fact that Sakurai uses silicide regions 107b for one transistor and does not utilize such silicide regions for another transistor is irrelevant to the claimed invention, as the claimed invention is referring to different silicide regions and more particularly to silicide regions that are between portions of the sidewall spacers and the substrate.

Further, Applicants respectfully disagree that the previous claim language of independent claim 29 was product by process. Notwithstanding this position, the final phrase of independent claim 29 has been amended to more clearly define structure and avoid process limitations.

Therefore, even if one ordinarily skilled in the art had combined Hellig with Sakurai as suggest in the Office Action, the proposed combination would not teach or suggest the claimed structure where the "silicide regions are larger in said first-type transistors than in said second-type transistors" as defined by independent claims 1, 8, and 29 especially since the silicide regions comprise "regions between portions of said sidewall spacers and said substrate."

Thus, Applicants submit that independent claims 1, 8, and 29 are not taught or suggested

by the prior art of record and independent claims 1, 8, and 29 are patentable over the prior art of record. Further, dependent claims 2, 4-7, 9, 11-14, and 30-33 are similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also by virtue of the additional features of the invention they define. In view of the foregoing, Applicants respectfully request that the Examiner reconsider and withdrawn this rejection.

II. Formal Matters and Conclusion

In view of the foregoing, Applicants submit that claims 1, 2, 4-9, 11-14 and 29-33, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary.

Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0458.

Respectfully submitted,

Dated: 4/6/05

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